WHAT IS CLAIMED IS:

1. A method of forming an isolation structure, the method comprising:

providing a substrate having a trench formed therein, the trench having at least one rounded corner;

applying a first nitride-containing liner on the substrate;

removing a portion of first nitride-containing liner such that a portion of the first liner remains within the trench and rounded corner; and

filling trench with a trench-filling material to form the isolation structure.

2. The method of claim 1, wherein the step of providing a substrate includes:

applying a mask layer to the substrate;

patterning the mask layer such that the patterned mask layer defines the trench;

etching the mask layer and the substrate to form the trench in the substrate; and

removing the mask layer.

3. The method of claim 2, wherein mask layer comprises a silicon nitride mask layer.

4. The method of claim 2 and further comprising rounding the corners of the trench after etching the substrate.

5. The method of claim 4, wherein rounding the corners of the trench comprises rounding the corners by annealing the substrate in a gaseous ambient.

6. The method of claim 4, wherein rounding the corners of the trench comprises rounding the corners by annealing the substrate in a gaseous ambient comprised of a gas selected from the group consisting of hydrogen, nitrogen, helium, neon, argon, and xenon, and combinations thereof.

7. The method of claim 4, wherein rounding the corners of the trench comprises rounding the corners by annealing the substrate in a gaseous ambient, wherein the annealing is performed at a temperature about 700 and about 950 degrees Celsius.

8. The method of claim 4, wherein rounding the corners of the trench comprises rounding the corners by annealing the substrate in a gaseous ambient, wherein the annealing is performed at a pressure of about 1 Torr to about 1000 Torr.

9. The method of claim 4, wherein rounding the corners of the trench comprising creating rounded corners having a radius of curvature of about 5 nm to about 50 nm.

10. The method of claim 1, wherein the first liner comprises Si_3N_4.

11. The method of claim 1 wherein the first liner comprises silicon oxynitride.

12. The method of claim 1, wherein the first liner has a nitrogen content about 5 to about 60 percent.

13. The method of claim 1, wherein the first liner has a thickness in the range of about 5 to about 200 angstroms.

14. The method of claim 1, wherein the trench-filling material is a dielectric.

15. The method of claim 14, wherein the trench-filling material comprises silicon oxide.

16. The method of claim 1, further comprising planarizing the trench-filling material.

17. The method of claim 16, wherein the planarizing step is a chemical mechanical polishing step.

18. The method of claim 1, further comprising forming transistors in close proximity to the trench.

19. The method of claim 1, further comprising:

forming transistors on the substrate in close proximity to the trench;

depositing an inter-layer dielectric over the transistors; and

depositing a metal line on the said inter-layer dielectric.

20. The method of claim 19 wherein the inter-layer dielectric comprises silicon oxide.

21. The method of claim 19 wherein the said metal line comprises a metal selected from the group consisting of aluminum, copper, and tungsten.

22. A method of forming an isolation structure, the method comprising:

providing a substrate having a trench formed therein and a patterned mask thereon, the patterned mask overlies portions of the substrate adjacent to the trench;

etching a portion of the patterned mask to pull-back the patterned mask from an edge of the trench;

annealing the substrate in a gaseous ambient to form rounded corners on the trench;

forming a nitrogen-containing liner over the trench and the patterned mask;

filling the trench with a trench-filling material;

removing a portion of nitrogen-containing liner overlying the patterned mask; and

removing the patterned mask.

23. The method of claim 22 and further comprising forming transistors on the substrate in close proximity to the trench.

24. The method of claim 22 and further comprising:

forming transistors in a region of the substrate adjacent to the trench;

forming an inter-layer dielectric over the transistors; and

forming a metal line over the inter-layer dielectric.

25. The method of claim 24 wherein the inter-layer dielectric comprises silicon oxide.

26. The method of claim 24 wherein the metal line comprises of a metal selected from the group consisting of aluminum, copper, and tungsten.

27. The method of claim 22, wherein the patterned mask comprises of a silicon nitride layer overlying a silicon dioxide layer.

28. The method of claim 22 wherein the rounded corners have a radius of curvature about 5 to about 50 nm.

29. The method of claim 22 wherein the annealing step is performed at a temperature of about 700 to about 950 degrees Celsius.

30. The method of claim 22, wherein the gaseous ambient comprises of hydrogen, nitrogen, helium, neon, argon, or xenon, or any combinations thereof.

31. The method of claim 22, wherein the annealing is performed at a pressure about 1 to 1000 Torr.

32. The method of claim 22, wherein the nitrogen-containing liner is comprised of silicon nitride or silicon oxynitride.

33. The method of claim 22, wherein the nitrogen-containing liner has a nitrogen content about 5 to 60 percent.

34. The method of claim 22, wherein the nitrogen-containing liner has a thickness about 5 to 200 angstroms.

35. The method of claim 22, wherein the trench-filling material is a dielectric.

36. The method of claim 22, wherein the trench-filling material comprises silicon oxide.

37. The method of claim 22, further comprising planarizing to remove a portion of the trench-filling material.

38. The method of claim 22, further comprising planarizing to remove a portion of the trench-filling material, wherein the planarizing is performed by chemical mechanical polishing.

39. A method of forming an isolation structure, the method comprising:

providing a semiconductor substrate having a top surface and having a trench formed therein, the trench having rounded corners in a top portion and having rounded corners in a bottom portion;

forming nitrogen-containing liner over the trench and the top surface;

filling the trench with a trench-filling material;

planarizing the trench-filling material such that the nitrogen-containing liner remains; and

removing the nitrogen-containing liner overlying the top surface.

40. The method of claim 39 and further comprising forming transistors in a region of the semiconductor substrate adjacent to the trench.

41. The method of claim 40 and further comprising:

forming an inter-layer dielectric over the transistors; and

forming a metal line on the inter-layer dielectric.

42. The method of claim 41 wherein the said inter-layer dielectric comprises of silicon oxide.

43. The method of claim 41 wherein the said metal line comprises of a metal selected from a group comprising of aluminum, copper, and tungsten.

44. The method of claim 39, wherein the rounded corners have a radius of curvature in the range of about 5 to about 50 nm.

45. The method of claim 39, wherein providing the substrate includes:

forming a patterned mask over the semiconductor substrate;

forming a trench in a portion of the semiconductor substrate not covered by the patterned mask;

removing the patterned mask; and

annealing the substrate in a gaseous ambient to form the rounded corners.

46. The method of claim 45 wherein annealing the substrate is performed at a temperature in the range of about 700 to about 950 degrees Celsius.

47. The method of claim 45 wherein the gaseous ambient comprises hydrogen, nitrogen, helium, neon, argon, or xenon, or any combinations thereof.

48. The method of claim 45 wherein annealing the substrate is performed at a pressure in the range of about 1 Torr to about 1000 Torr.

49. The method of claim 39 and further comprising forming a silicon dioxide liner prior to forming the nitrogen-containing liner.

50. The method of claim 39, wherein the nitrogen-containing liner comprises of silicon nitride or silicon oxynitride.

51. The method of claim 39, wherein the nitrogen-containing liner has a nitrogen content of about 5 to about 60 percent.

52. The method of claim 39, wherein the nitrogen-containing liner has a thickness in the range of about 5 to about 200 angstroms.

53. The method of claim 39, wherein the trench-filling material is a dielectric.

54. The method of claim 53, wherein the trench-filling material comprises silicon oxide.

55. The method of claim 39, wherein planarizing the trench-filling material is performed by a chemical mechanical polishing process.

56. The method of claim 55 wherein the chemical mechanical polishing process employs a slurry comprising of cerium oxide.

57. An isolation structure comprising:

a substrate having a trench with sidewall surfaces and at least one of a top rounded corner and a bottom rounded corner;

a nitrogen-containing liner in contact with at least one of the top rounded corner or the bottom rounded corner; and

a trench-filling material in the trench.

58. The structure of claim 57, wherein the top rounded corner or bottom rounded corner has a radius of curvature in the range of about 5 to about 50 nm.

59. The structure of claim 57, wherein the trench has a trench depth in the range of about 2000 to about 6000 angstroms.

60. The structure of claim 57, wherein the nitrogen-containing liner has a thickness in the range of about 5 to about 200 angstroms.

61. The structure of claim 57, further comprising of at least one transistor formed in a portion of the substrate adjacent to the trench.

62. The structure of claim 57, wherein the trench-filling material comprises silicon oxide.

63. The structure of claim 57, wherein the trench-filling material comprises poly-crystalline silicon.

64. The structure of claim 57, wherein the nitrogen-containing liner comprises silicon nitride.

65. The structure of Claim 57 wherein the nitrogen containing liner comprises silicon oxynitride.

66. The structure of claim 57, wherein the nitrogen-containing liner has a nitrogen content of about 5 to about 60 percent.

67. An semiconductor structure comprising:

a semiconductor substrate having a trench with a sidewall surface;

a nitrogen-containing liner in contact with the sidewall surface;

a trench-filling material in the trench;

an active area within the semiconductor substrate, the active area having at least one transistor device formed therein;

an inter-layer dielectric overlying said semiconductor substrate;

a metal line overlying said inter-layer dielectric; and

a conductive contact connecting the metal line to the active area.

68. The structure of claim 67 wherein the trench has a trench depth in the range of about 2000 to about 6000 angstroms.

69. The structure of claim 67 wherein the nitrogen-containing liner has a thickness in the range of about 5 to about 200 angstroms.

70. The structure of claim 67, wherein the trench-filling material comprises silicon oxide.

71. The structure of claim 67, wherein the trench-filling material comprises silicon oxide.

72. The structure of claim 67, wherein the trench-filling material comprises poly-crystalline silicon.

73. The structure of claim 67, wherein the nitrogen-containing liner comprises silicon nitride.

74. The structure of claim 67, wherein the nitrogen-containing liner comprises silicon oxynitride.

75. The structure of claim 67, wherein the nitrogen-containing liner has a nitrogen content of about 5 to about 60 percent.

76. The structure of claim 67, wherein the inter-layer dielectric comprises silicon oxide.

77. The structure of claim 67, wherein the metal line comprises a metal selected from the group consisting of aluminum, copper, and tungsten.